INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO - 1449	ATTORNEY DOCKET NO. 00791/LH	SERIAL NO. 09/704,156
	APPLICANT: Takeshi WAKABAYASHI	
	FILED: November 1, 2001	ART UNIT: 2814

U.S. PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB	
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		08-070081	03/1996	Japan			X*	
		11-121507	04/1999	Japan			X*	
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OTHER DOCUMENTS (AUTHOR, TITLE, DATE, PAGES, PUBLICATION, ETC.)

LT	Masatoshi YASUNAGA et al: "CHIP SCALE PACKAGE* (CSP) A LIGHTLY DRESSED LSI CHIP", Proceedings of the IEEE/CPMT International Electronics Manufacturing Technology Symposium, New York, U.S., IEEE Vol. Symp. 16, pages 169-176 XP000530088, ISBN: 0-7803-2038-7, page 169 - page 171; Figures 1-6.

EXAMINER: Luan Thai	DATE CONSIDERED: 1/31/02

*English language Abstract only.

March 7, 2001